DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

Structures and methods for memory cells having a volatile and a non-volatile component in a single memory cell are provided. The memory cell includes a first source/drain region and a second source/drain region separated by a channel region in a substrate. A storage capacitor is coupled to one of the first and the second source/drain regions. A floating gate opposes the channel region and separated therefrom by a gate oxide. A control gate opposes the floating gate. The control gate is separated from the floating gate by a low tunnel barrier intergate insulator. The memory cell is adapted to operate in a first and a second mode of operation. The first mode of operation is a dynamic mode of operation and the second mode of operation is a repressed memory mode of operation.